PRODUCT DETAILS

25G SFP28-Duplex Optical Transceiver

QD1310-SFP-LC.S10

Single-Mode, 1310nm, 25G SFP28-Duplex With LC interface

Product Description

The QD1310-SFP-LC.S10 optical transceiver is designed for fiber communication application up to 25.78Gbps, with CDR engaged, while, 10G Ethernet optical data communication can be supported when CDR is bypassed. It is with the SFP+ 20-pin connector to allow hot plug capability. Digital diagnostic functions are available via an I^2C.

The QD1310-SFP-LC.S10 has built-in clock and data recovery (CDR). This module is designed for single-mode fiber and operates at wavelength of 1310nm.The transmitter is wavelength 1310nm multiple quantum well
DFB laser and is a class 1 laser compliant according to International Safety Standard IEC 60825. The receiver section uses an integrated InGaAs detector preamplifier (IDP) mounted in an optical header and a limiting post-amplifier IC.

Features

- Operating data rate support 24.33Gbps and 25.78Gbps with CDR engaged mode
- Operating data rate support 9.95Gbps and 10.31Gbps with CDR bypassed mode
- 1310nm Uncooled DFB Transmitter
- Single 3.3V power supply
- Power dissipation <1.2W for Standard
- Power dissipation <1.5W for Industrial
- Distance up to 10km
- Duplex LC connector interface
- Built-in dual CDR
- Compliant with MSA SFP+ Specification SFF-8402
- Operating case temperature range:
  Standard: 0°C to 70°C
  Industrial: -40°C to 85°C
- RoHS compliant (lead-free)
- I^2C interface with integrated Digital Diagnostic Monitoring
- Safety Certification: TUV/UL/FDA*1

Applications

- CPRI Option 10
- 25GbE
- Other Optical Link

Ordering Information

Part No.	Data Rate	Laser	Distance	Interface	Temp.	DDMI
QD1310-SFP-LC.S10 *2	Up to 25.78Gbps	Uncooled DFB	10km	LC/SMF	0~70°C	Yes

QD1310-SFP-LC.S10(WT)*3	Up to 25.78Gbps	Uncooled DFB	10km	LC/SMF	-40~85℃	Yes

*1: For the latest certification information, please check with Data Controls Inc. *2: Standard version. *3: Industrial version.

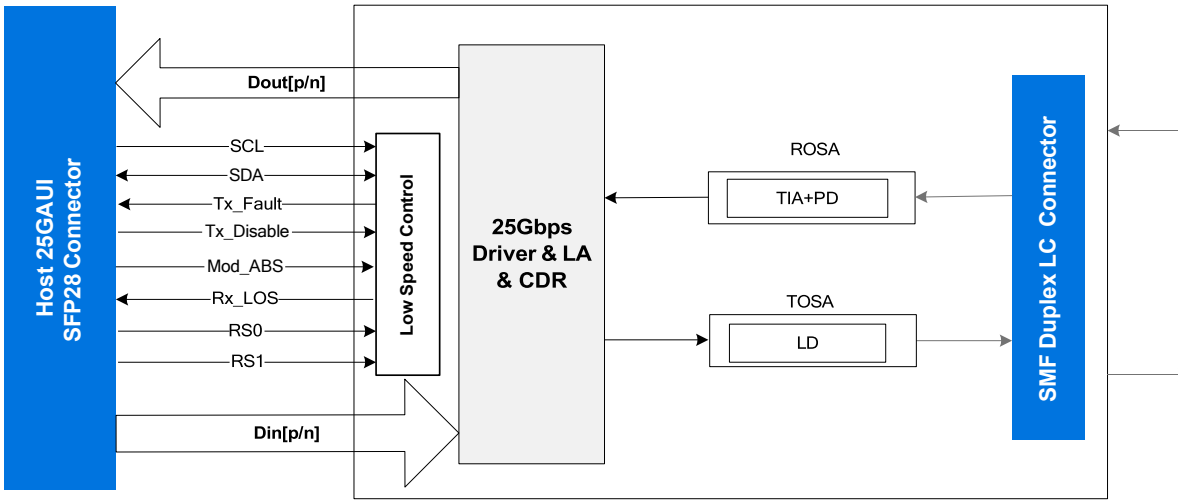

Figure 1: Transceiver Block Diagram

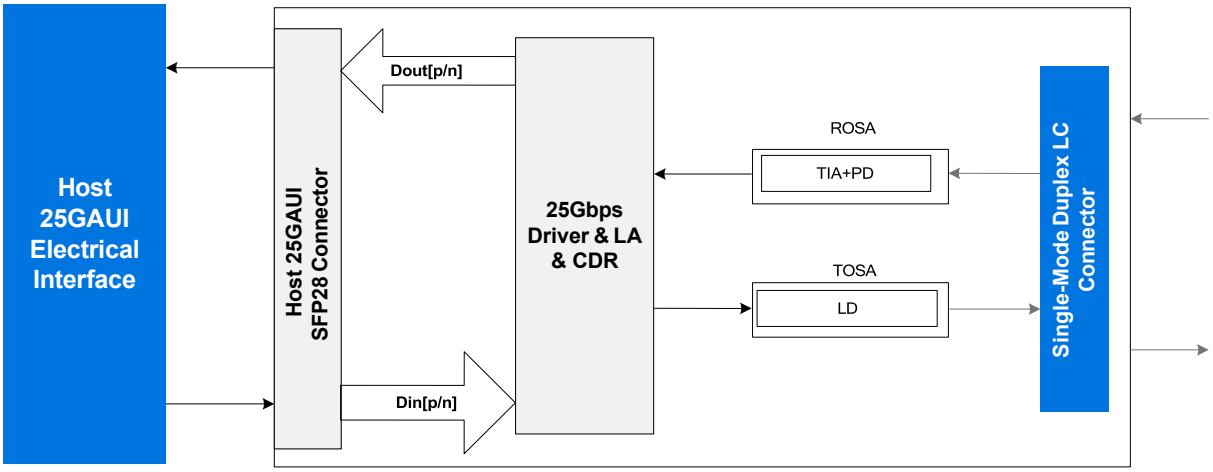

Figure 2: Application Reference Diagram

Transmitter

As show in Figure 1, the optical transmitter portion of the transceiver incorporates a 25GAUI electrical input with Equalization (EQ) block, DFB laser driver, diagnostic monitors, control and bias for the modulator. The QD1310-SFP-LC.S10 transmitter section uses a wavelength of 1310nm uncooled DFB laser.

Receiver

As show in Figure 1, the optical receiver portion of the transceiver incorporates the PD photodiode, trans-impedance amplifiers (TIA) and 25GAUI compliant electrical output blocks. The Rx Output Buffer provides 25GAUI compliant differential outputs for the high speed electrical interface.

High Speed Electrical Signal Interface

The interface between the SFP28 module and ASIC/SerDes is showed in Figure 2. The high speed signal lines are internally AC-coupled and the electrical inputs are internally terminated to 100 Ohms differential. Both transmitter and receiver electrical channels are compliant to module 25GAUI specification.

Low Speed Electrical Signal Interface

The module has the following low speed signals for control and status: TX_Fault, TX_Disable, MOD_ABS, RX LOS, RS0, RS1. In addition, there is an industry standard two wire serial interface scaled for 3.3V LVCMOS. It is implemented as a slave device. Signal and timing characteristics are further defined in the Control Characteristics and Control Interface.

Handling and Cleaning

Exposure to current surges and overvoltage events can cause immediate damage to the transceiver module. Observe the precautions for normal operation of electrostatic discharge sensitive equipment; Attention shall also be paid to limiting transceiver module exposure to conditions beyond those specified in the absolute maximum ratings.

Optical connectors include female connectors. These elements will be exposed as long as the cable or port plug is not inserted. At this time, always pay attention to protection.

Each module is equipped with a port guard plug to protect the optical port. The protective plug shall always be in place whenever the optical fiber is not inserted. Before inserting the optical fiber, it is recommended to clean the end of the optical fiber connector to avoid contamination of the module optical port due to dirty connector. If contamination occurs, use standard LC port cleaning methods.

Absolute Maximum Ratings

Exceeding the absolute maximum ratings table may cause permanent damage to the device. This is just an emphasized rating, and does not involve the functional operation of the device that exceeds the specifications of this technical specification under these or other conditions. Long-term operation under absolute maximum ratings will affect the reliability of the device.

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage Temperature	Ts	-45		100	℃
Power Supply Voltage	Vcc	-0.5	3.3	4.0	V
Relative Humidity (Non Condensing)	RH	5		85	%

Recommended Operating Conditions*4

For operations beyond the recommended operating conditions, optical and electrical characteristics are not defined, reliability is not implied, and such operations for a long time may damage the module.

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature (Standard)*5	Tc	0		70	°C
Operating Case Temperature (Industrial)*5	Tc	-40		85	°C
Power Supply Voltage	Vcc	3.135	3.3	3.465	V
Power Supply Noise *6				25	mVpp
Receiver Differential Data Output Load			100		Ohm
Fiber Length (SMF)				10	km

*4：Power Supply specifications, Instantaneous, sustained and steady state current compliant with SFP28 MSA Power Classification.

*5: The position of case temperature measurement is shown in Figure 9.

*6: Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 7 for recommended power supply filter.

General Electrical Characteristics*7

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Symbol	Min.	Typical	Max.	Unit
Transceiver Power Consumption (Standard)				1.2	W
Transceiver Power Consumption (Industrial)				1.5	W
Transceiver Power Supply Total Current (Standard)				360	mA
Transceiver Power Supply Total Current (Industrial)				455	mA
AC Coupling Internal Capacitor			0.1		uF

*7: For control signal timing including TX_Fault, TX_Disable, MOD-ABS, RX LOS, RS0, RS1, SCL and SDA see Control Interface Section.

Reference Points

Test Point	Description
TP1 and TP4	TP1 and TP4 are informative reference points that may be useful to implementers for testing components
TP2	Unless specified otherwise, all transmitter measurements and tests defined in 802.3cc 114.5
TP3	Unless specified otherwise, all receiver measurements and tests defined in 802.3cc 114.5.

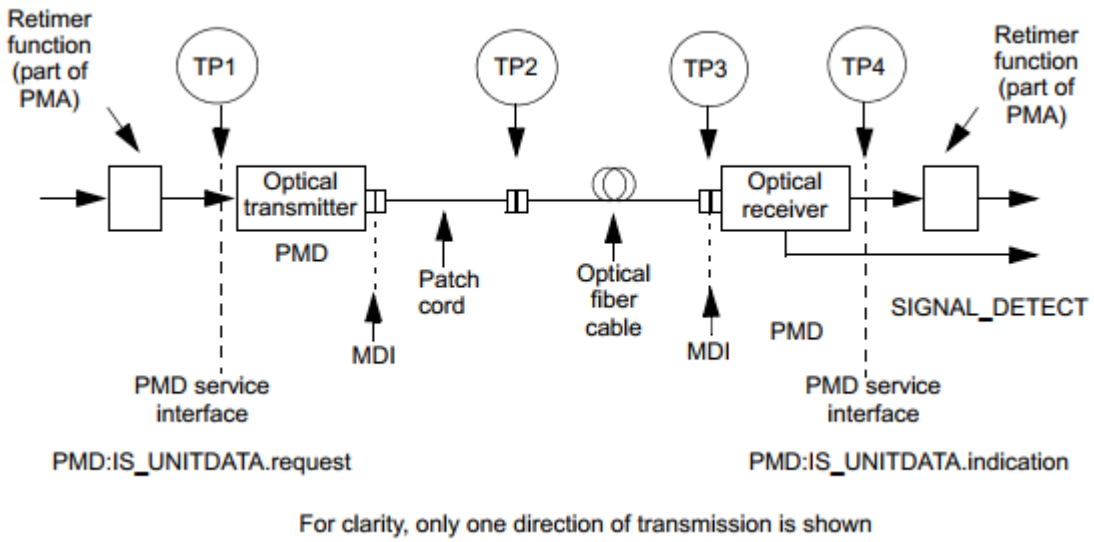

Figure 3: IEEE 802.3cc block diagram for 25GBASE LR transmit/Receive paths

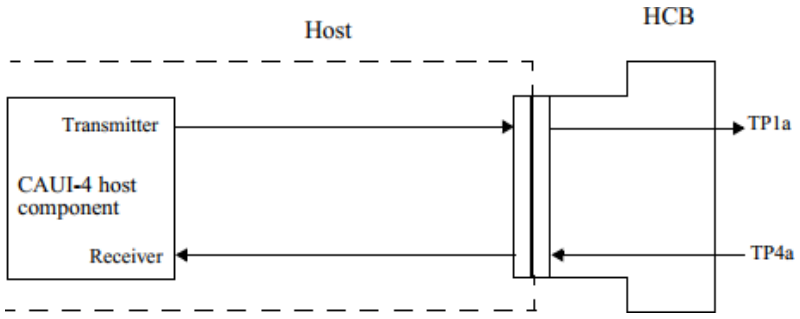

Figure 4: IEEE 802.3 25GAUI compliance points TP1a, TP4a

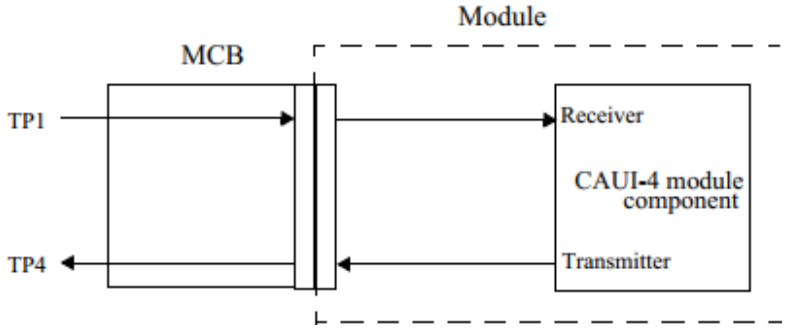

Figure 5: IEEE 802.3 25GAUI compliance points TP1, TP4

High Speed Electrical Input Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Test Point	Min.	Typical	Max.	Unit	Standards
Signaling Rate Per Lane	TP1		25.78125+/- 100 ppm		GBd	
DC Common-Mode Voltage*8	TP1	-350		2850	mV	
AC Common-Mode output Voltage(RMS)	TP1a			17.5	mV	
Differential peak-peak input Voltage Tolerance	TP1a	900			mV	
Single-Ended Voltage Tolerance Range	TP1a	-400		3300	mV	
Differential Input Return Loss	TP1	Equation (83E-5)			dB	802.3
Differential to Common Mode Input Return Loss	TP1	Equation (83E-6)			dB	802.3
Differential Termination Mismatch	TP1			10	%	
Transition time(20% to 80%)	TP1a	10			ps	
Module Stressed Input Test*9			83E.3.4.1			
Eye Width	TP1a	0.46			UI	
Eye Height	TP1a	95			mV	
Applied peak-peak Sinusoidal Jitter	TP1a		Table 88-13			802.3

*8: DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

*9: Module stressed input tolerance is measured using the procedure defined in 83E.3.4.1.

High Speed Electrical Output Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Test Point	Min.	Typical	Max.	Unit
Signaling Rate Per Lane (Range)	TP4a		25.78125 ± 100 ppm		GBd
Common Mode Voltage	TP4a	-0.3		2.8	V
AC Common-Mode output Voltage(RMS)	TP4			17.5	mV
Differential peak-peak Output Voltage	TP4			900	mV
Differential Input Return Loss	TP4a	Equation (83E-5)			dB
Differential To Common Mode Input Return Loss (Min)	TP4a	Equation (83E-6)			dB
Differential Termination Mismatch	TP4a			10	%
Transition time(20% to 80%)	TP4	12			ps
Host Stressed Input Test			83E3.3.2		
Eye Width	TP4	0.57			UI
Eye Height	TP4	228			mV

High Speed Optical Transmitter Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

25GBASE-LR Optical Characteristics @TP2 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling Speed			25.78125 ± 100ppm		GBd
Modulation Format			NRZ		
Center Wavelength	λ	1295	1310	1325	nm
Spectral Width (-20dB)				1	nm
Side-mode suppression ration	SMSR	30			dB
Extinction Ratio	ER	3.0			dB
Average Launch Power		-7		2	dBm
Outer Optical Modulation Amplitude (OMA)		-4		2.2	dBm
Launch power in OMA minus TDP		-5			dBm
Transmitter Dispersion Penalty	TDP			2.7	dB
$Rin_{20}OMA$				-130	dB/Hz
Average Launch Power Of OFF Transmitter				-20	dBm
Optical Return Loss Tolerance				20	dB
Transmitter reflectance				-26	dB
Transmitter eye mask definition{X1,X2,X3,Y1,Y2,Y3} Hit ratio $5x10^{-5}$ hits per sample			{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}		

High Speed Optical Receiver Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

25GBASE-LR Optical Characteristics @TP3 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling Speed Per Lane			25.78125 ± 100ppm		GBd
Modulation Format			NRZ		
Center Wavelength	λ1	1295	1310	1325	nm
Damage Threshold		3			dBm
Average Receiver Power Per Lane		-13.3		2	dBm
Receiver Power (OMA)				2.2	dBm
Receive Sensitivity (OMA)*10	Sen_{OMA}			-12	dBm
Stressed Receiver Sensitivity (OMA)				-9.5	dBm
Conditions of stressed receiver sensitivity test					
Stressed eye closure			2.5		dB
Stressed eye J2 jitter			0.27		UI
Stressed eye J4 jitter			0.39		UI
SRS eye mask definition {X1,X2,X3,Y1,Y2,Y3} Hit ratio 5 $x10^{-5}$ hits per samples			{0.31,0.4,0.45,0.34,0.38,0.4}		
Los Assert (Avg.)	LOSA	-30			dBm
Los De-Assert (Avg.)	LOSD			-15	dBm
Receiver Reflectance				-26	dB

*10: Measured with PRBS31 at BER=5E-5, 25.78Gb/s.

Regulatory Compliance Issues

Various standard and regulations apply to the QD1310-SFP-LC.S10 modules. These include eye-safety, Component Recognition, RoHS, ESD, EMC and Immunity. Please note the transmitter module is a Class 1 laser product. See Regulatory Compliance Table for details.

Regulatory Compliance Table

Feature	Test Method	Performance
Laser Eye Safety and Equipment Type Testing 	(IEC) EN 62368-1:2014+A11 (IEC) EN 60825-1:2014 (IEC) EN 60825-2:2004+A1+A2	CDRH Accession Number:2132182-000 TUV File: R 50457725 0001 CB File: JPTUV-100513
Component Recognition	Underwriters Laboratories (UL) and Canadian Standards Association (CSA) Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File: E317337
RoHS Compliance	RoHS Directive 2011/65/EU& (EU)2015/863	Less than 100 ppm of cadmium. Less than 1000 ppm lead, mercury, hexavalent chromium, poly brominated biphenyls (PPB), poly brominated biphenyl ethers (PBDE), dibutyl phthalate, butyl benzyl phthalate, bis (2-ethylhexyl) phthalate and diisobutyl phthalates.
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM)	High speed contacts shall withstand 1000V. All other contacts shall withstand 2000 V.
Electrostatic Discharge (ESD) to the Optical Connector Receptacle	IEC 61000-4-2:2008	When installed in a properly grounded housing and chassis the units are subjected to 15kV air discharges during operation and 8kV direct discharges to the case.
Electromagnetic Interference (EMI)	FCC Part 15 Class B; CISPR 32 (EN55032) 2015;	System margins are dependent on customer board and chassis design.
Immunity	IEC 61000-4-3:2010; EN55035:2017	Typically shows no measurable effect from a 10V/m field swept from 80 MHz to 6 GHz applied to the module without a chassis enclosure.

Electrostatic Discharge (ESD)

The QD1310-SFP-LC.S10 is complies with the ESD requirements described in the Regulatory Compliance Table. However, in the normal processing and operation of optical transceiver, the following two types of situations need special attention.

Case I: Before inserting the transceiver into the rack meeting the requirements of SFP28 MSA, ESD preventive measures must be taken to protect the equipment. For example, the grounding wrist strap, workbench and floor should be used wherever the transceiver is handled.

Case II: After the transceiver is installed, the electrostatic discharge outside the chassis of the host equipment shall be within the scope of system level ESD requirements. If the optical interface of the transceiver is exposed outside the host equipment cabinet, the transceiver may be subject to equipment system level ESD requirements.

Electromagnetic Interference (EMI)

Communication equipment with optical transceivers is usually regulated by FCC in the United States and CENELEC EN55032 (CISPR 32) in Europe. The compliance of QD1310-SFP-LC.S10 with these standards is detailed in the regulatory compliance table. The metal shell and shielding design of QD1310-SFP-LC.S10 will help equipment designers minimize the equipment level EMI challenges they face.

Flammability

QD1310-SFP-LC.S10 optical transceiver meets UL certification requirements, its constituent materials have heat and corrosion resistance, and the plastic parts meet UL94V-0 requirements.

SFP28 Transceiver Electrical Pad Layout

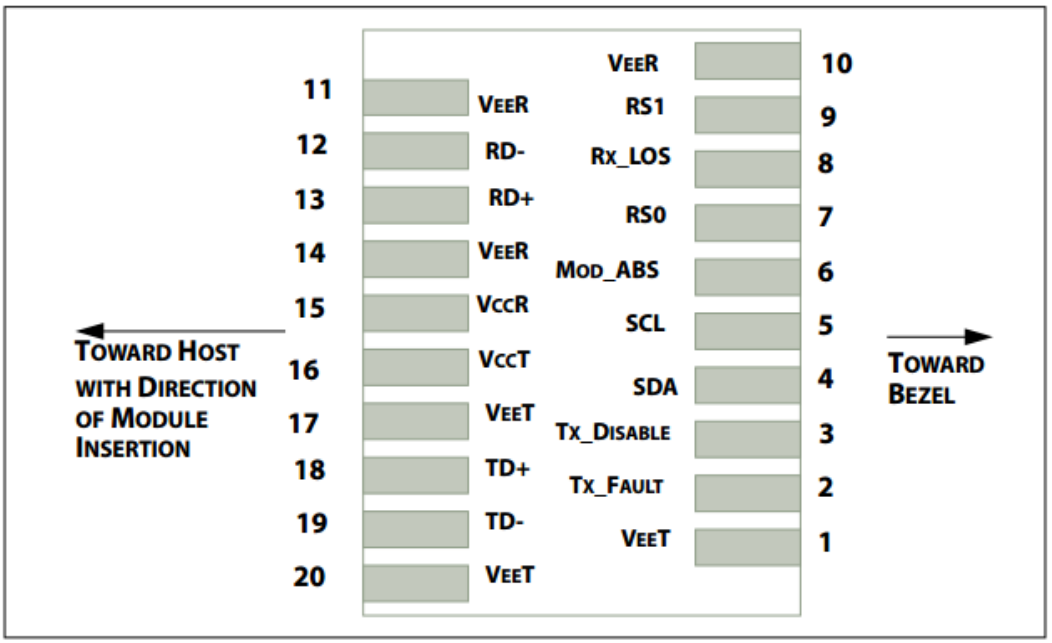

Figure 6: SFP28 Module Pinout

Pin Arrangement and Definition

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		VeeT	Transmitter Ground	1	3
2	LVTTL-O	Tx_Fault	Transmitter Fault Indication	3	4
3	LVTTL-I	Tx_Disable	Transmitter Disable	3	5
4	LVTTL-I/O	SDA	2-Wire Serial Interface Data Line	3	6
5	LVTTL-I/O	SCL	2-Wire Serial Interface Clock	3	6
6		Mod_ABS	Module Absent	3	7
7	LVTTL-I	RS0	Rate Select 0	3	8
8	LVTTL-I/O	Rx_LOS	Receiver Loss of Signal Indication	3	4
9	LVTTL-I	RS1	Rate Select 1	3	8
10		VeeR	Receiver Ground	1	3
11		VeeR	Receiver Ground	1	3
12	CML-O	RD-	Receiver Inverted Data Output	3	
13	CML-O	RD+	Receiver Non-Inverted Data Output	3	
14		VeeR	Receiver Ground	1	3
15		VccR	Receiver 3.3V Supply	2	
16		VccT	Transmitter 3.3V Supply	2	
17		VeeT	Transmitter Ground	1	3
18	CML-I	TD+	Transmitter Data Input	3	
19	CML-I	TD-	Transmitter Inverted Data Input	3	
20		VeeT	Transmitter Ground	1	3

1. Labeling as inputs (I) and outputs (O) are from the perspective of the module
2. The case makes electrical contact to the cage before any of the board edge contacts are made.
3. The module signal ground contacts, VeeR and VeeT, should be isolated from the module case.
4. This contact is an open collector/drain output contact and shall be pulled up on the host see 2.4.1 and 2.4.6. Pull ups can be connected to one of several power supplies, however the host board design shall ensure that no module contact has voltage exceeding module VccT/R +0.5 V.
5. Tx_Disable is an input contact with a 4.7 kΩ to 10 kΩ pullup to VccT inside the module.
6. See SFF-8431 4.2.
7. See SFF-8431 2.4.4.
8. For SFF-8431 rate select definition see section 2.4.3 and 2.5.

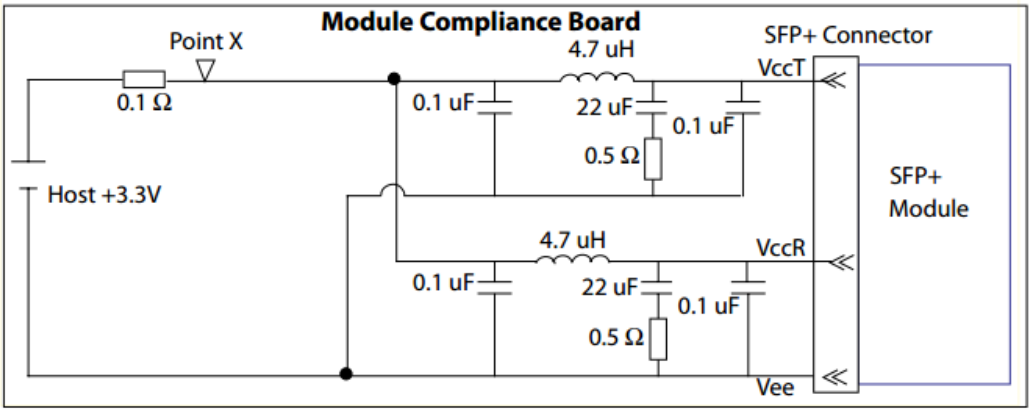

Figure 7: Host Board Power Supply Filter

Package Outline

The module is designed to meet the package outline defined in the SFP28 MSA specification. See the package outline for details.

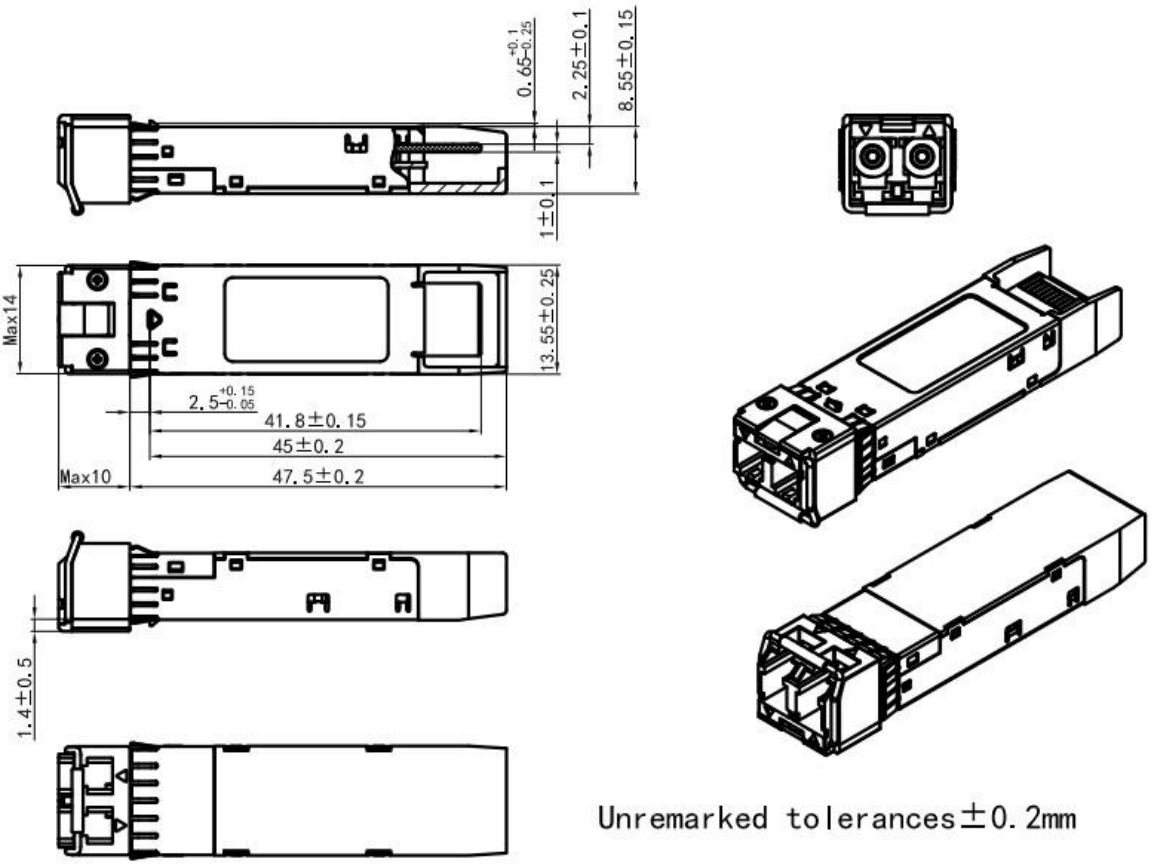

Figure 8: Mechanical Package Outline (All dimensions in mm)

*This 2D drawing is only for reference, please check with Data Controls Inc before ordering.

The bellow picture shows the location of the hottest spot for measuring module case temperature. In addition, the digital diagnostic monitors (DDM) temperature is also calibrated to this spot.

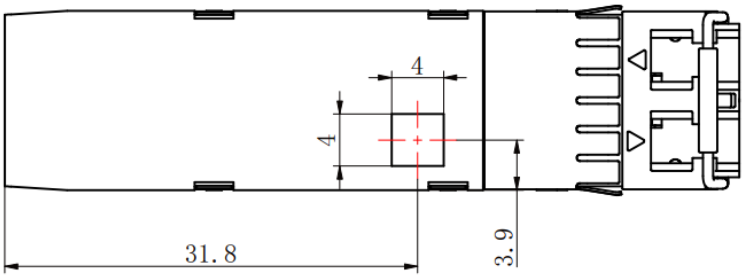

Figure 9: Case Temperature Measurement Point (All dimensions in mm)

The optical interface port is a Duplex LC connector.

Figure 10: Module Optical Interface (looking into the optical port)

Control Interface & Memory Map

The control interface combines dedicated signal lines for TX Fault, TX Disable, MOD-ABS, RX LOS, RS0, RS1 with two-wire serial (TWS), interface clock (SCL) and data (SDA), signals to provide users rich functionality over an efficient and easily used interface.

SCL and SDA

SCL and SDA are a 2-wire serial interface between the host and module using the I2C protocols. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host.

SCL and SDA Pin Electrical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit
SCL and SDA	VOL	0		0.4	V
	VOH	VCC-0.5		VCC+0.3	V
SCL and SDA	VIL	-0.3		VCC*0.3	V
	VIH	VCC*0.7		VCC+0.5	V

Tx_Fault

Tx_Fault is a module output that when high, indicates that the module transmitter has detected a fault condition related to laser operation or safety. If Tx_Fault is not implemented, the Tx_Fault contact signal shall be held low by the module and may be connected to Vee within the module.
The Tx_Fault output is an open drain/collector and shall be pulled up to the Vcc_Host in the host with a resistor in the range 4.7 kΩ to 10 kΩ, or with an active termination according to SFF-8431 Table 6.

Tx_Disable

When Tx_Disable is asserted high or left open, the SFP+ module transmitter output shall be turned off unless the module is a passive cable assembly in which case this signal may be ignored. This contact shall be pulled up to VccT with a 4.7 kΩ to 10 kΩ resistor in modules and cable assemblies. Tx_Disable is a module input contact.
When Tx_Disable is asserted low or grounded the module transmitter is operating normally.

RS0/RS1

RS0 and RS1 are module inputs and are pulled low to VeeT with > 30 kΩ resistors in the module. The QD1310-SFP-LC.S10 support high data rates 24.33G/25.78G (CPRI options 10 /25GbE) and Low data rates 9.95G/10.31G (10GbE).

Logic OR of RS0 Pin and Bit110.3 of A2H	Logic OR of RS1 Pin and Bit118.3 of A2H	RX Data Rate	TX Data Rate	Status of RX CDR	Status of TX CDR
High/1	High/1	24.33G/25.78G	24.33G/25.78G	CDR Engaged	CDR Engaged
High/1	Low/0	24.33G/25.78G	9.95G/10.31G	CDR Engaged	CDR Bypassed
Low/0	High/1	9.95G/10.31G	24.33G/25.78G	CDR Bypassed	CDR Engaged
Low/0	Low/0	9.95G/10.31G	9.95G/10.31G	CDR Bypassed	CDR Bypassed

Mod_ABS

Mod_ABS is connected to VeeT or VeeR in the SFP+ module. The host may pull this contact up to Vcc_Host with a resistor in the range 4.7 kΩ to 10 kΩ.
Mod_ABS is asserted “High” when the SFP+ module is physically absent from a host slot. In the SFP MSA (INF-8074i) this contact has the same function but is called MOD_DEF0.

Rx_LOS

Rx_LOS high indicates an optical signal level below that specified in the relevant standard. Rx_LOS is an open drain/collector output, but may also be used as an input by supervisory circuitry in the module. For a nominally 3.3 V Vcc_Host using a resistive pull up to Vcc_Host, the resistor value shall be in the range of 4.7 kΩ to 10 kΩ.

Memory Map

The Module provides diagnostic information about the present operating conditions. The transceiver generates this diagnostic data by digitization of internal analog signals. Calibration and alarm/warning threshold data is written during device manufacture. Received power monitoring, transmitted power monitoring, bias current monitoring, supply voltage monitoring and temperature monitoring all are implemented. The digital diagnostic memory map specific data field defined as following. This part is compliant with SFF-8472 Rev12.2.

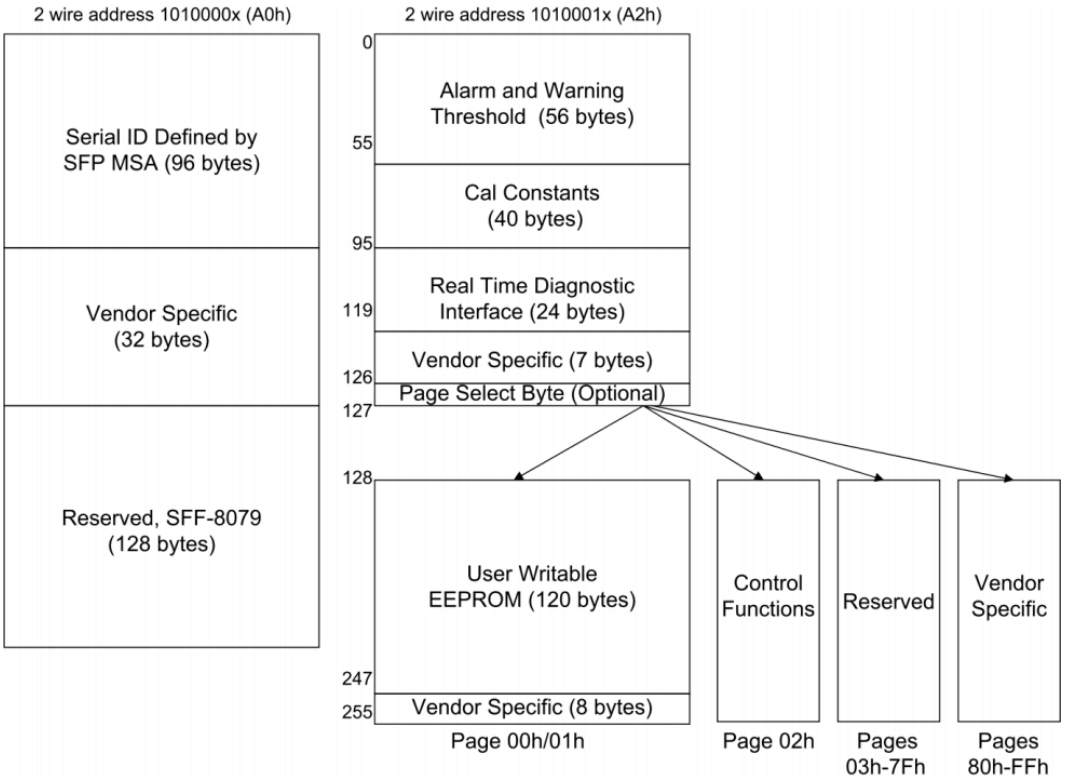

Figure 11: 2-wire Interface Fields

Revision History

Revision	Revision History	Release Date
V3.a	New Template Version.	Oct 20, 2023
V3.b	Update Characteristics of TP1 and TP4 based on IEEE802.3.	Oct 27, 2023

Quality

Data Controls Inc has passed many quality system verifications, established an internationally standardized quality assurance system and strictly implemented standardized management and control in the course of design, development, production, installation and service. For latest certification/accreditation numbers, please, contact us.

Notice

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Contact:
Data Controls Inc.
8F VORT Asakusabashi Ekimae Bldg V, 1-20-4 Yanagibashi,
Taito-ku , Tokyo 111-0052, JAPAN | TEL:+81-3-5829-5805
Email: info@dci.jp https://www.dci.jp