100G BIDI 40km QSFP28 Optical Transceiver

HB1305-QSF-LC.S40
HB1310-QSF-LC.S40

Single-Mode, 100G QSFP28With LC interface

Product Description

Data Controls Inc.'s Single Lambda QSFP28 BIDI transceiver module is designed for use in 100 Gigabit Ethernet links over 40km single mode fiber. The module incorporates 1 channel optical signal, operating at 100Gbps data rate. This module can convert 4 channels of 25Gbps (NRZ) electrical input data to 1 channel of 100Gbps (PAM4) optical signal, and also can convert 1 channel of 100Gbps (PAM4) optical signal to 4 channels of 25Gbps (NRZ) electrical output data. The electrical interface of the module is compliant with the OIF CEI-28G-VSR and QSFP28 MSA.

Features

- Supports 100Gbps
- 100G Lambda MSA 100G-ER1 SpecificationCompliant
- Single 3.3V Power Supply
- Power Dissipation < 4.5W
- Up to 40km over SMF with inbuild KP4 FEC
- QSFP28 MSA Compliant
- SFF-8636 Rev 2.10a Compliant
- 4x25G Electrical Interface
- BIDI LC receptacles
- Commercial Case Temperature Range of0°C to +70°C
- I2C Interface with Integrated DigitalDiagnostic Monitoring
- Safety Certification: TUV/UL/FDA*1
- RoHS Compliant

Applications

- 100G Ethernet
- Data center

Ordering Information

Part No.	Data Rate	Wavelength (Tx)	Fiber	Distance*2	Latch Color	Interface	Temp.
HB1305-QSF-LC.S40	100Gbps	1304.58nm	SMF	40km	Blue	LC	0~+70°C
HB1310-QSF-LC.S40	100Gbps	1309.14nm	SMF	40km	Green	LC	0~+70°C

*1: For the latest certification information, please check with Data Controls Inc..
*2: Over G.652 SMF.

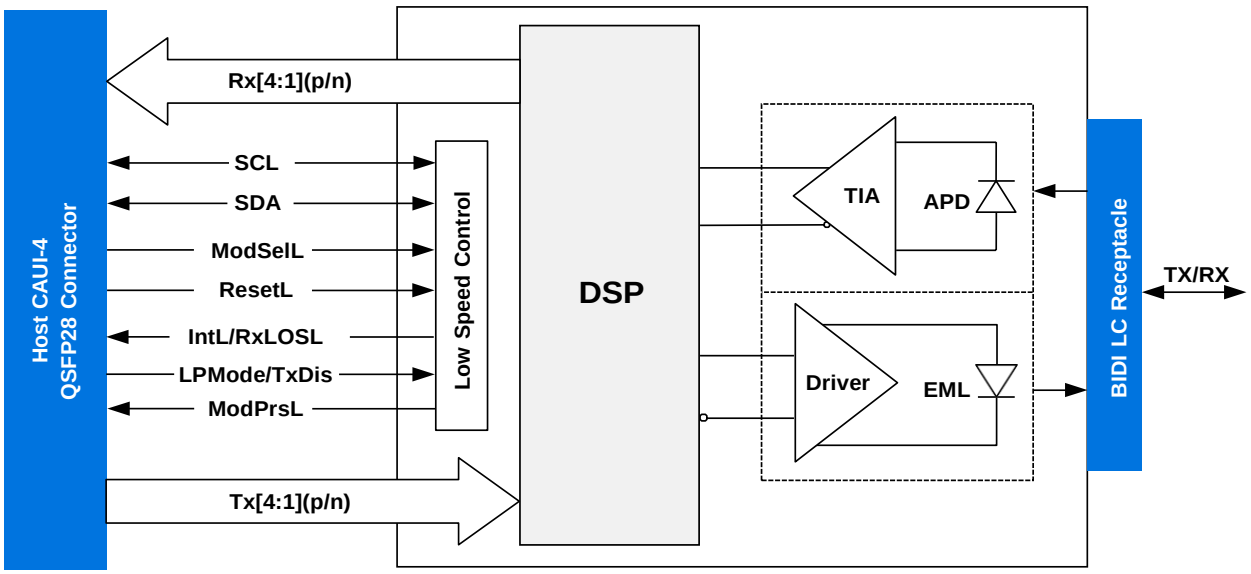

Figure 1: Transceiver Block Diagram

Only one channel *i* (*i*=1, 2, 3, 4) shown for simplicity

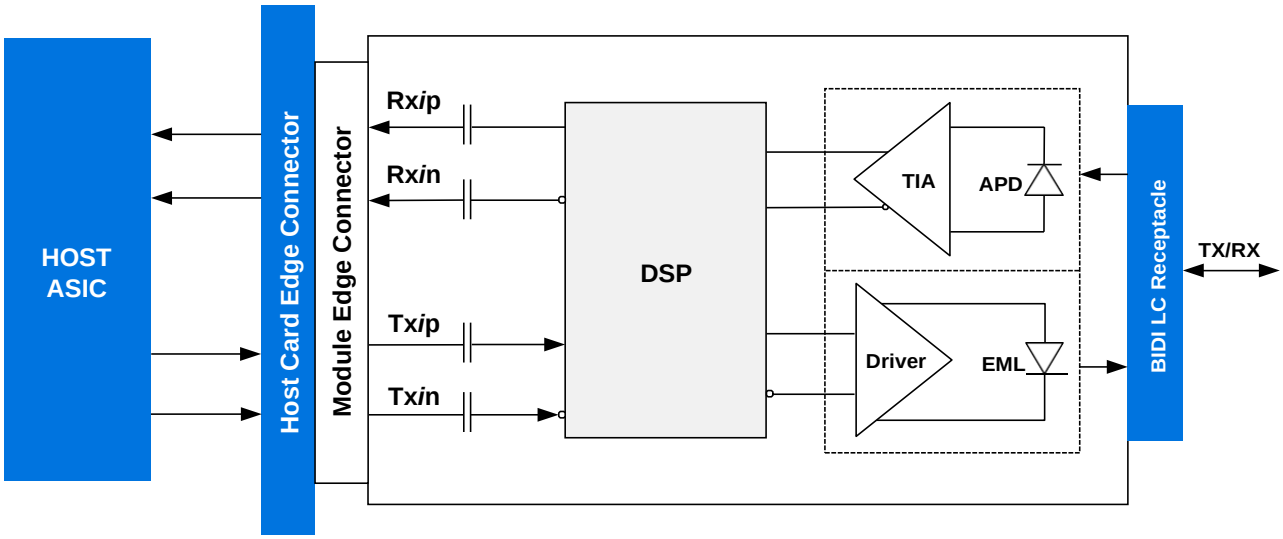

Figure 2: Application Reference Diagram

Transmitter

As shown in Figure 1, the transmitter path of the transceiver contains a 4x25Gbps CAUI-4 electrical input, integrated electrical multiplexer, EML driver, EML Laser and diagnostic monitor. The integrated electrical multiplexer converts 4 channels of 25Gbps (NRZ) electrical input data to 1 channel of 100Gbps (PAM4) optical signal.

Receiver

As shown in Figure 1, the receiver path of the transceiver contains an APD, trans-impedance amplifier (TIA), integrated de-multiplexer and 4x25Gbps CAUI-4 compliant electrical output block. The integrated de-multiplexer converts 1 channel of 100Gbps (PAM4) optical signal to 4 channels of 25Gbps (NRZ) electrical output data.

High Speed Electrical Signal Interface

The interface between QSFP28 module and ASIC/SerDes is showed in Figure 2. The high speed signal lines are internally AC-coupled and the electrical inputs are internally terminated to 100 Ohms differential. All transmitter and receiver electrical channels are compliant to CAUI-4 specification per IEEE 802.3cd.

Control Signal Interface

The module has the following low speed signals for control and status: ModSelL, ResetL, LPMode/TxDis, ModPrsL, IntL/RxLOSL. In addition, there is an industry standard two wire serial interface scaled for 3.3V LVTTL. The definition of control signal interface and the registers of the serial interface memory are further defined in the Control Interface& Memory Map section

Handling and Cleaning

Exposure to current surges and overvoltage events can cause immediate damage to the transceiver module. Observe the precautions for normal operation of electrostatic discharge sensitive equipment, and attention should also be taken to restrict exposure to the conditions defined in the absolute maximum ratings.

Optical connectors will be exposed as long as the port plug is not inserted, so always pay attention to protection. Each module is equipped with a port guard plug to protect the optical ports. The protective plug shall always be in place whenever the optical fiber is not inserted. Before inserting the optical fiber, it is recommended to clean the end of the optical fiber connector to avoid contamination of the module optical port due to dirty connector. If contamination occurs, use standard LC port cleaning methods.

Absolute Maximum Ratings

Exceeding the absolute maximum ratings table may cause permanent damage to the device. This is just an emphasized rating, and does not involve the functional operation of the device that exceeds the specifications of this technical specification under these or other conditions. Long-term operation under absolute maximum ratings will affect the reliability of the device.

Parameter	Symbol	Min.	Max.	Unit
Storage temperature	Ts	-40	+85	°C
Operating case temperature	Tc	-5	75	°C
Supply voltage	Vcc	-0.5	3.6	V
Damage threshold	Rxdmg	-2.4		dBm

Recommended Operating Conditions*3

For operations beyond the recommended operating conditions, optical and electrical characteristics are not defined, reliability is not implied, and such operations for a long time may damage the module.

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating case temperature*4	Tc	0		70	°C
Power supply voltage	Vcc	3.135	3.3	3.465	V
Operating relative humidity	RH	5		85	%

Power dissipation	P_D		4.5	W
Electrical signal rate		25.78125		Gbps
Optical signal rate		53.125		Gbaud
Power supply noise *5			66	mVpp
Receiver differential dataoutput load		100		Ohm
Fiber length (9μm SMF) *6			40	km

*3: Power supply specifications, instantaneous, sustained and steady state current are compliant with QSFP28 MSA powerclassification.

*4: The position of case temperature measurement is shown in Figure 9.

*5: Power supply noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 7 for recommended power supply filter.

*6: 9μm SMF. The maximum link distance is based on an allocation of 1dB of attenuation and 3dB total connection and splice loss. The loss of a single connection shall not exceed 0.5dB.

General Electrical Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Min.	Typical	Max.	Unit
Transceiver power consumption			4.5	W
Transceiver power supply current, Total			1298	mA
AC coupling capacitors (Internal)		0.1		μF

Reference Points

Reference point	Description
TP0	Host ASIC transmitter output at ASIC package contact.
TP1	Input to module compliance board through mated module compliance board and module connector. Used to test module input.
TP1a	Host ASIC transmitter output through the host board and host card edge connector at the output of the host compliance board. Also used to calibrate module input compliance signals.
TP4	Module output through the compliance board connectors at the output of the module compliance board. Also used to calibrate host input compliance signals.
TP4a	Input to host compliance board. Used to test host input.
TP5	Input to host ASIC.
TP5a	Far end module output through a reference channel.

Note: Individual standards may specify unique reference points.

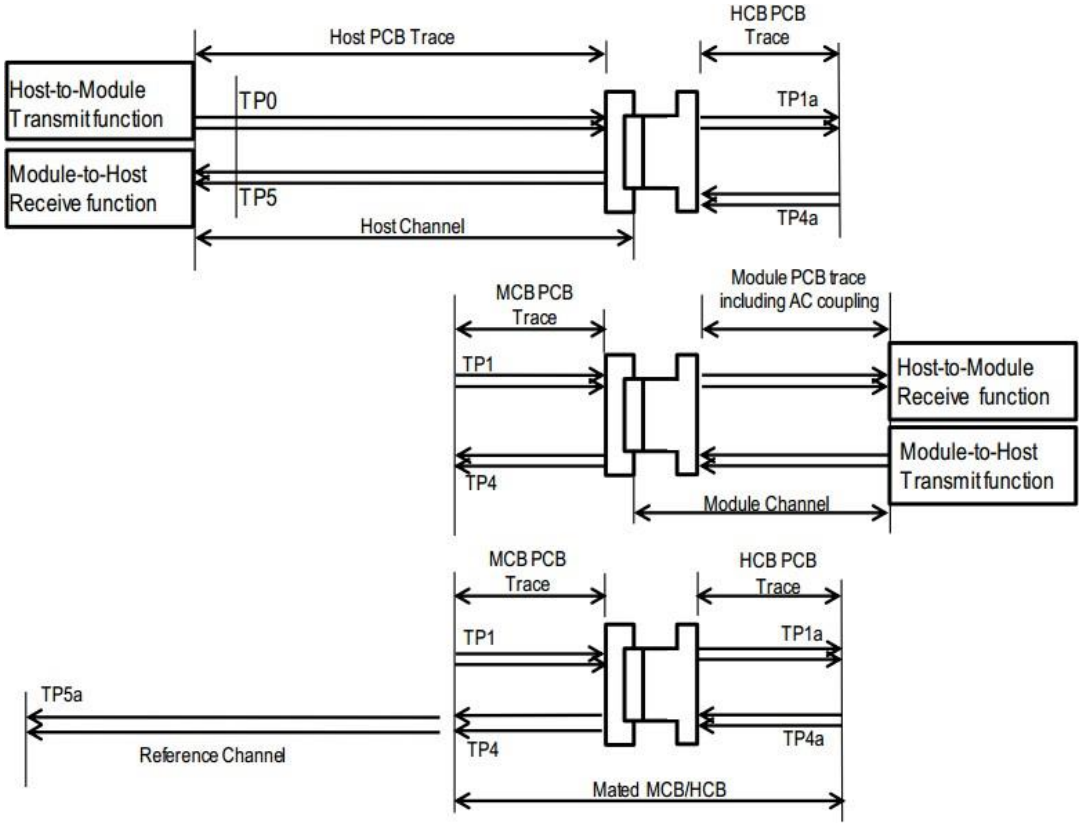

Figure 3: Reference points and compliance boards

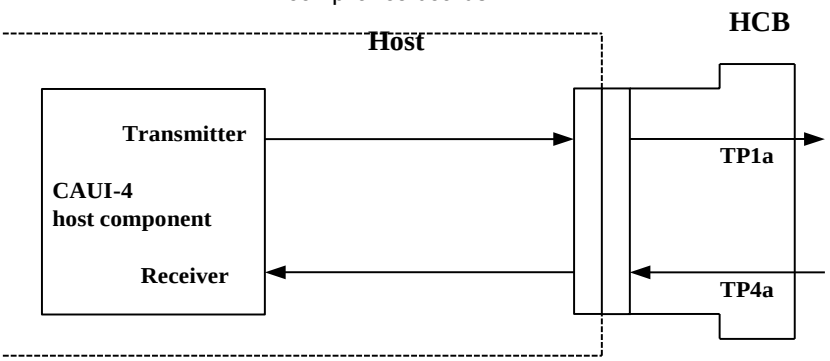

Figure 4: IEEE 802.3 CAUI-4 compliance points TP1a, TP4a

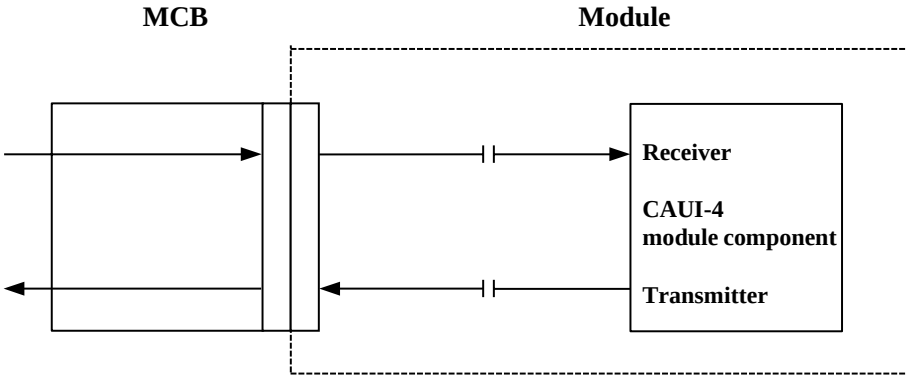

Figure 5: IEEE 802.3 CAUI-4 compliance points TP1, TP4

High Speed Electrical Input Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Test Point	Min.	Typical	Max.	Unit	Conditions
Transmitter						
Differential peak-peak input voltage tolerance	TP1a	900			mV_{p-p}	
Differential input impedance	TP1	90	100	110	Ohm	
Output rise/fall time	TP1a	10			ps	20%~80%
Eye width	TP1a	0.46			UI	1E-15
Eye height , differential	TP1a	95			mV	1E-15
DC common mode voltage (V_{cm}) *7	TP1	-350		2850	mV	

High Speed Electrical Output Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Test Point	Min.	Typical	Max	Unit	Conditions
Differential peak-peak output voltage	TP4			900	mV_{p-p}	
Differential output impedance	TP4	90	100	110	Ohm	
Output rise/fall time	TP4	12			ps	20%~80%
Eye width	TP4	0.57			UI	1E-15
Eye height differential	TP4	228			mV	1E-15
DC common mode voltage (V_{cm}) *7	TP4	-350		2850	mV	

*7: V_{cm} is generated by the host. Specification includes effects of ground offset voltage.

High Speed Optical Transmitter Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Optical Characteristics @TP2 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Transmitter					
Signaling speed			53.125		Gbaud
Modulation format			PAM4		
Center wavelength (HB1305-QSF-LC.S40)	λc	1304.06	1304.58	1305.1	nm
Center wavelength (HB1310-QSF-LC.S40)		1308.61	1309.14	1309.66	
Side-mode suppression ratio	SMSR	30			dB
Extinction ratio	ER	5			dB
Outer optical modulation amplitude for TDECQ<1.4dB for 1.4dB≤TDECQ≤3.9dB	TxOMA	4.7 3.3+TDECQ		7.9	dBm
Transmit average*8	TxAVG	1.7		7.1	dBm
Transmitter and dispersion eye closure	TDECQ			3.9	dB
Launch power of OFF Transmitter per lane				-15	dBm
Relative Intensity Noise	RIN			-136	dB/Hz
Optical return loss tolerance				15	dB
Transmitter reflectance*9				-26	dB

*8: Average launch power (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

*9: Transmitter reflectance is defined looking into the transmitter.

High Speed Optical Receiver Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Optical Characteristics @TP3 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling speed			53.125		Gbaud
Center wavelength (HB1305-QSF-LC.S40)	λC	1308.61	1309.14	1309.66	nm
Center wavelength (HB1310-QSF-LC.S40)		1304.06	1304.58	1305.1	
Damage threshold	Rxdmg	-2.4			dBm
Receive power (OMA_{outer})	RxOMA			-2.6	dBm
Average receive power	RxAVG	-16		-3.4	dBm
Receiver sensitivity (OMA_{outer})*10 for TECQ<1.4dB for 1.4dB≤TECQ≤3.9dB	SenOMA			-13.8 TECQ-15.2	dBm
Stressed receiver sensitivity	SRS			-11.3	dBm

Receiver reflectance			-26	dB
Los Assert	LOSA	-26		dBm
LOS De-Assert	LOSD		-17	dBm

*10: Sensitivity is specified at $2.4x10^{-4}$ BER with PRBS31Q.

Regulatory Compliance

Various standard and regulations apply to the HB1305-QSF-LC.S40/ HB1310-QSF-LC.S40 modules. These include Eye-Safety, Component Recognition, RoHS, ESD, EMC and Immunity. Please note the transmitter module is a Class 1 laser product. See regulatory compliance table for details.

Regulatory Compliance Table

Feature	Test Method	Performance
Laser Eye Safety and Equipment Type Testing 	(IEC) EN 62368-1:2014+A11 (IEC) EN 60825-1:2014 (IEC) EN 60825-2:2004+A1+A2	CDRH Accession Number:2132182-000 TUV File: R 50457725 0001 CB File: JPTUV-100513
Component Recognition	Underwriters Laboratories (UL) and Canadian Standards Association (CSA) Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File: E317337
RoHS Compliance	RoHS Directive 2011/65/EU&(EU)2015/863	Less than 100 ppm of cadmium. Less than 1000 ppm lead, mercury, hexavalent chromium, poly brominated biphenyls (PPB), poly brominated biphenyl ethers (PBDE), dibutyl phthalate, butyl benzyl phthalate, bis (2-ethylhexyl) phthalate and diisobutyl phthalates.
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM)	High speed contacts shall withstand 1000V. All other contacts shall withstand 2000 V.
Electrostatic Discharge (ESD) to the Optical Connector Receptacle	IEC 61000-4-2:2008	When installed in a properly grounded housing and chassis the units are subjected to 15kV air discharges during operation and 8kV direct discharges to the case.
Electromagnetic Interference	FCC Part 15 Class B;	System margins are dependent on

(EMI)	CISPR 32 (EN55032) 2015;	customer board and chassis design.
Immunity	IEC 61000-4-3:2010; EN55035:2017	Typically shows no measurable effect from a 10V/m field swept from 80 MHz to 6 GHz applied to the module without a chassis enclosure.

Electrostatic Discharge (ESD)

The HB1305-QSF-LC.S40/HB1310-QSF-LC.S40 modules comply with the ESD requirements described in the regulatory compliance table. However, in the normal processing and operation of optical transceiver, the following two types of situations need special attention.

Case I: Before inserting the transceiver into the rack meeting the requirements of QSFP28 MSA, ESD preventive measures must be taken to protect the equipment. For example, the grounding wrist strap, workbench and floor should be used wherever the transceiver is handled.

Case II: After the transceiver is installed, the electrostatic discharge outside the chassis of the host equipment shall be within the scope of system level ESD requirements. If the optical interface of the transceiver is exposed outside the host equipment cabinet, the transceiver may be subject to equipment system level ESD requirements.

Electromagnetic Interference (EMI)

Communication equipment with optical transceivers is usually regulated by FCC in the United States and CENELEC EN55032 (CISPR 32) in Europe. The compliance of HB1305-QSF-LC.S40/HB1310-QSF-LC.S40 with these standards is detailed in the regulatory compliance table. The metal shell and shielding design of HB1305-QSF-LC.S40/HB1310-QSF-LC.S40 will help equipment designers minimize the equipment level EMI challenges they face.

Flammability

The HB1305-QSF-LC.S40/HB1310-QSF-LC.S40 optical transceiver meets UL certification requirements, its constituent materials have heat and corrosion resistance, and the plastic parts meet UL94V-0 requirements.

QSFP28 Transceiver Electrical Pad Layout

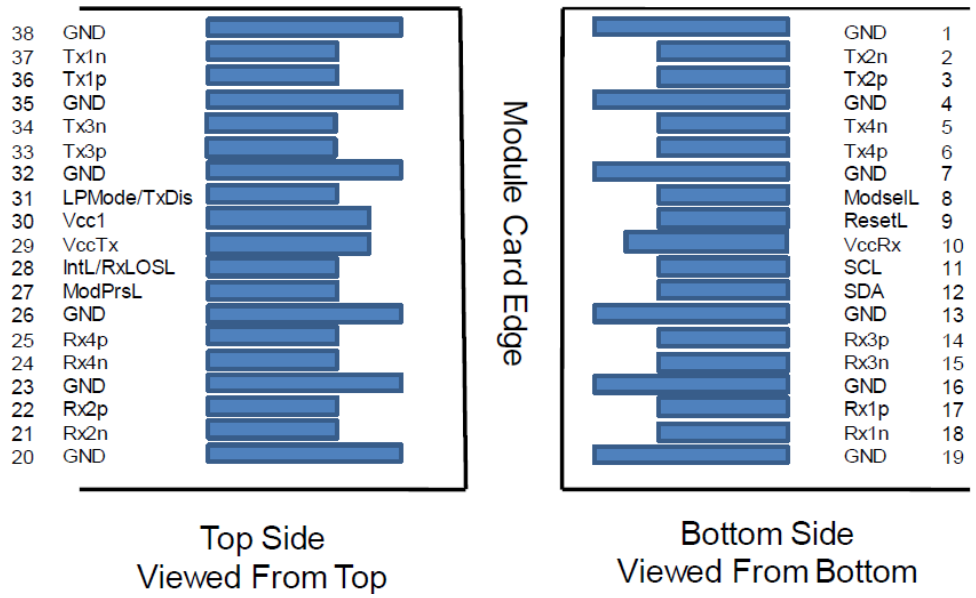

Figure 6: QSFP28 Module Pinout

Pin Arrangement and Definition

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS- I/O	SCL	Two-wire serial interface clock	3	
12	LVCMOS- I/O	SDA	Two-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1

20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/ RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636).	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode/ TxDis	Low Power Mode. Optionally configurable as TxDis via the management interface (SFF-8636).	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect them directly to the host board signal-common ground plane.

Note 2: VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and applied concurrently. VccRx, Vcc1 and VccTx are internally connected within the module in any combination. Vcc contacts in SFF-8662 and SFF-8672 each have a steady state current rating of 1A.

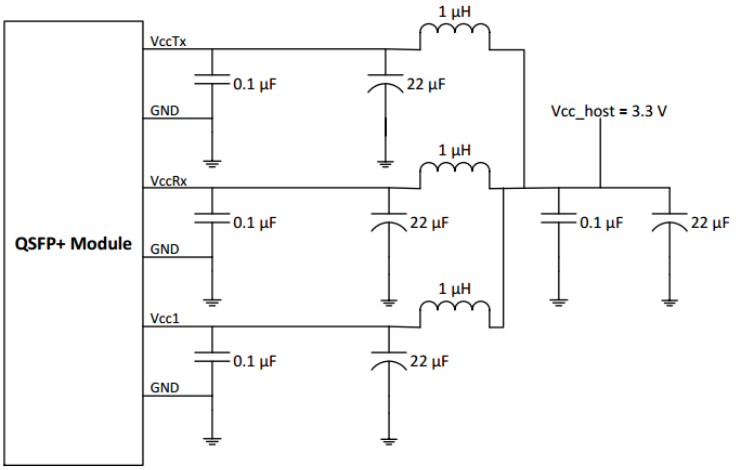

Figure 7: Host Board Power Supply Filter

During power transient events, the host should ensure that any neighboring modules sharing the same

supply stay within their specified supply voltage limits. The host should also ensure that the intrinsic noise of the power rail is filtered in order to guarantee the correct operation of the optical modules.

Package Outline

The module is designed to meet the package outline defined in the QSFP28 MSA specification. See thepackage outline for details.

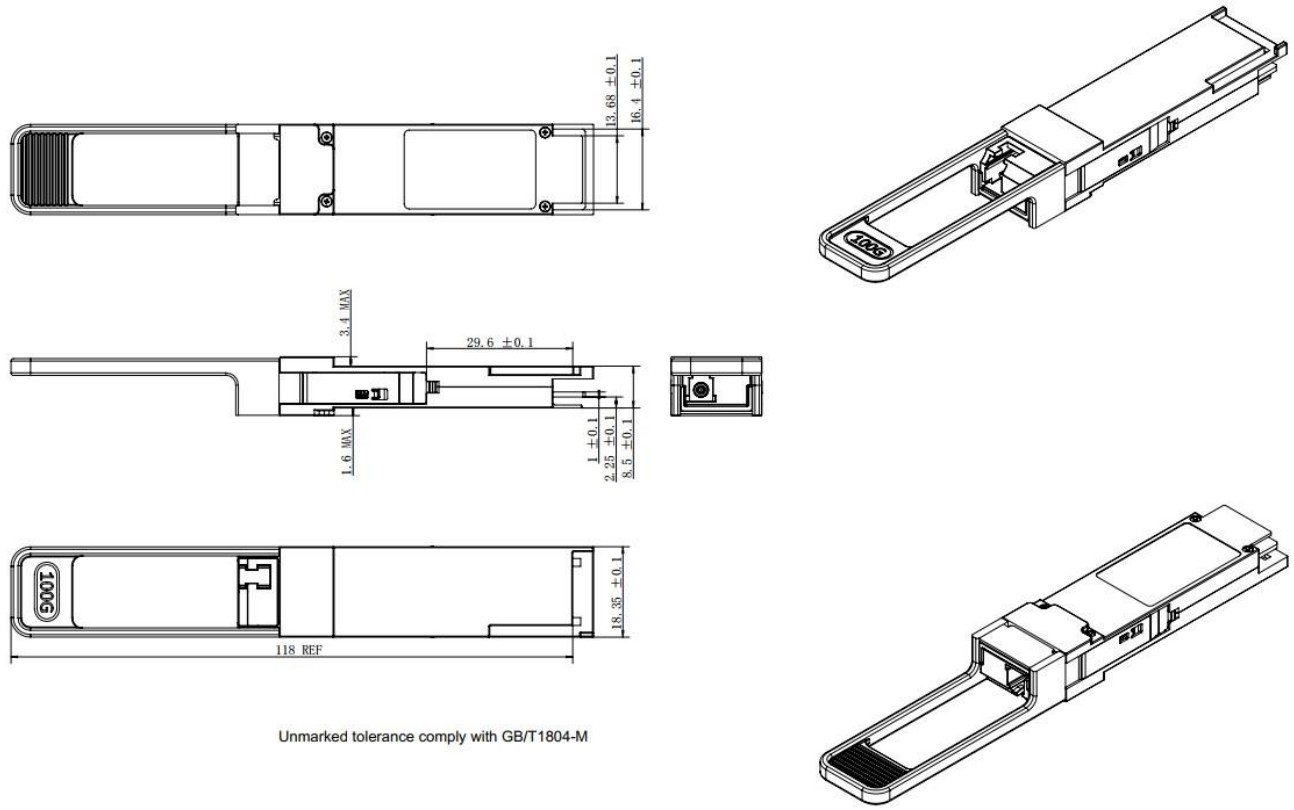

Figure 8: Mechanical Package Outline (All dimensions in mm)

*This 2D drawing is only for reference, please check with Data Controls Inc. before ordering.

The bellow picture shows the location of the hottest spot for measuring module case temperature. Inaddition, the digital diagnostic monitors (DDM) temperature is also calibrated to this spot.

Figure 9: Case Temperature Measurement Point (All dimensions in mm)

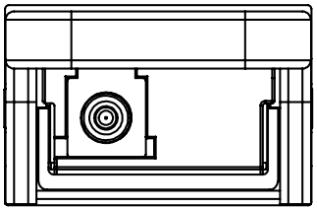

Figure 10: Module Optical Interface (looking into the optical port)

Control Interface & Memory Map

The control interface combines dedicated signal lines for ModSelL, ResetL, LPMode/TxDis, ModPrsL, IntL/RxLOSL, two-wire serial interface clock (SCL) and data (SDA), signals to provide users rich functionality over an efficient and easily used interface.

ModSelL

ModSelL is an input signal. When held low by the host, the module responds to two-wire serial communication commands. When ModSelL is high, the module can't respond to or acknowledge any two-wire interface communication from the host. The ModSelL signal input node is pulled up towards Vcc in the module with a resistor of 10kΩ. In order to avoid conflicts, the host system won't attempt two-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host will wait at least for the period of the ModSelL assert time before communicating with the newly selected module.

ResetL

The ResetL signal is pulled up towards Vcc in the module with a resistor of 10kΩ. A low level on ResetL for longer than 10μs initiates a complete module reset, returning all user module settings to their default state.

LPMode/TxDis

LPMode/TxDis is a dual-mode input signal from the host operating with active high logic. It is pulled up towards Vcc in the module with a resistor of 10kΩ. At power-up or after ResetL is de-asserted, the LPMode/TxDis behaves as LPMode. LPMode/TxDis can be configured as TxDis using the two-wire interface except during the execution of a reset.

When LPMode/TxDis is configured as LPMode, the module behaves as though TxDis=0. By using the LPMode signal and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits (SFF-8636, Address A0h, Byte 93 bits 0,1,2), the host controls how much power a module can consume.

When LPMode/TxDis is configured as TxDis, the module behaves as though LPMode=0. In this mode LPMode/TxDis when set to 1 or 0 disables or enables all optical transmitters within the times specified in SFF-8636.

Changing LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is high disables all optical transmitters. If the module was in low power mode, then the module transitions out of low power mode at the same time. If the module is already in high power state with transmitters already enabled, the

module will disable all optical transmitters.
Changing the LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is low simply changes the behavior of the mode of LPMode/TxDis. The behavior of the module depends on the Power Override control bits.

ModPrsL

ModPrsL is pulled up towards Vcc_Host on the host board and pulled towards ground in the module. ModPrsL is pulled low when inserted and released to high when it is physically absent from the host connector.

IntL/RxLOSL

IntL/RxLOSL is a dual-mode active-low, open-collector output signal from the module. It is pulled up towards Vcc on the host board with a resistor of 10kΩ. At power-up or after ResetL is released to high, IntL/RxLOSL is configured as IntL. IntL/RxLOSL can be optionally programmed as RxLOSL using the two-wire interface except during the execution of a reset.
If IntL/RxLOSL is configured as IntL, a low indicates a possible module operational fault or a module condition that sets an unmasked flag as defined in SFF-8636. The source of the IntL "low" can be read, cleared or masked using the two-wire interface. If the interrupt was after a module reset and SFF-8636, Page 00h, Byte 2, bit 0 (Data_Not_Ready bit) is 0, then the module releases IntL to high after the host has read the Data_Not_Ready bit. For all other interrupt causes, the module releases IntL to high after the host has read the flag associated with the cause of the interrupt.
If IntL/RxLOSL is configured as RxLOSL, a low indicates that there is a loss of received optical power on at least one lane, a high indicates that there is no loss of received optical power. The module pulls RxLOSL to low if any lane in a multiple lane module has a LOS condition and release RxLOSL to high only if no lane has a LOS condition.

SCL and SDA

The SCL and SDA is a hot plug interface that can support a bus topology. During module insertion or removal, the module will implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

Control Interface Electrical Specifications

Parameter	Symbol	Min.	Max.	Unit
SCL and SDA	VOL	0	0.4	V
	VOH	VCC-0.5	VCC+0.3	V
SCL and SDA	VIL	-0.3	VCC*0.3	V
	VIH	VCC*0.7	VCC+0.5	V
Capacitance on SCL and SDA I/O contact	Ci		14	pF
Total bus capacitive load for SCL and SDA	Cb		100	pF
			200	pF

LPMode/TxDis, ResetL and ModSelL	VIL	-0.3	0.8	V
	VIH	2	Vcc+0.3	V
	Iin	-365	125	µA
ModPrsL and IntL/RxLOSL	VOL	0	0.4	V
	VOH	Vcc-0.5	Vcc+0.3	V

Note: Positive values indicate current flowing into the module.

Memory Map

The memory is structured as a single address, multiple page approach and is compliant with the QSFP28 MSA. The module meets the following requirements:

1. The module initialize in hardware mode when LPMode is de-asserted.
2. The transmitter is disabled when the module is held in reset.
3. Tx Squelch function is implemented as defined by the QSFP28 MSA. When squelched, the transmitter remains on with the modulation turned off.
4. Rx Squelch function is implemented as defined by the QSFP28 MSA. When RxLOSL is asserted, the receiver output is squelched.

Register Overview

From	To	Content	No. of bytes	Type
		2-Wire Serial Address 1010000x		
		Lower Page 00h		
0	2	ID and Status	3	Read-Only
3	21	Interrupt Flags (Clear on read)	19	Read-Only
22	33	Free Side Device Monitors	12	Read-Only
34	81	Channel Monitors	48	Read-Only
82	85	Reserved	4	Read-Only
86	99	Control	14	Read/Write
100	106	Free Side Interrupt Masks	7	Read/Write
107	110	Free Side Device Properties	4	Read-Only
111	112	Assigned to PCI Express	2	Read/Write
113	116	Free Side Device Properties	4	Read-Only
117	118	Reserved	2	Read/Write
119	122	Optional Password Change	4	Write-Only
123	126	Optional Password Entry	4	Write-Only
127	127	Page Select Byte	1	Read/Write
		Upper Page 00h		
128	128	Identifier	1	Read-Only
129	191	Base ID Fields	63	Read-Only
192	223	Extended ID	32	Read-Only
224	255	Vendor Specific ID	32	Read-Only
		Page 01h (Optional)		

128	255	Reserved (previously for SFF-8079 support)	128	Read-Only
		Page 02h (Optional)		
128	255	User EEPROM Data	128	Read/Write
		Page 03h (Optional)		
128	175	Free Side Device Thresholds	48	Read-Only
176	223	Channel Thresholds	48	Read-Only
224	229	Tx EQ, Rx Output and TC Support	6	Read-Only
230	241	Channel Controls	12	Read/Write
242	251	Channel Monitor Masks	10	Read/Write
252	255	Reserved	4	Read/Write
		Pages 04h-1Fh (Optional)		
128	255	Vendor Specific	128	Read/Write
		Pages 20h-21h (Optional)		
128	255	PAM-4 and WDM Features	128	Read/Write
		Pages 22h-7Fh (Optional)		
128	255	Reserved	128	Read/Write
		Pages 80h-FFh (Optional)		
128	255	Vendor Specific	128	Read/Write

Revision History

Revision	Revision History	Release Date
V1.a	Preliminary	Aug 12, 2022
V1.b	Update transmit and receive characteristics.	Dec 06, 2022
V1.c	Add industrial-grade information.	Jun 19, 2023
V1.d	Delete industrial-grade information.	Jul 06, 2023

Quality

Data Controls Inc. has passed many quality system verifications, established an internationally standardized quality assurance system and strictly implemented standardized management and control in the course of design, development, production, installation and service. For latest certification/accreditation numbers, please, contact us.

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