

# **XFP Series**

# JCxxxx-XFP-LC.S40 Series

CWDM XFP Single-Mode for 10GbE/10GFC/SDH/SONET Duplex XFP Transceiver RoHS6 Compliant

#### **Features**

- Supports 9.95Gb/s to 11.1Gb/s Bit Rates
- Hot-Pluggable XFP Footprint
- Compliant with XFP MSA
- 8-Wavelengths CWDM EML Transmitter from 1470nm to 1610nm, with Step 20nm
- 14dB power budget at least
- Duplex LC Connector
- Power Dissipation < 3.5W</p>
- Case Operation Temperature
   Standard: 0°C to 70°C
  - Industrial:-40°C to 85°C
- 2-Wire Interface for Integrated Digital
   Diagnostic Monitoring



#### **Applications**

- SONET / SDH
- ◆ 10GBASE-ER/EW 10G Ethernet
- 1200-SM-LL-L 10G Fiber Channel
- 10GE over G.709 at 11.09Gbps
- OC192 over FEC at 10.709Gbps

## **Ordering Information**

Part No.	Data Rate	Laser	Fiber	Distance	Interface	Temp
JCxxxx-XFP-LC.S40*(note1)	10G	CWDM EML	SMF	14dB power budget	LC	Standard
JCxxxx-XFP-LC.S40(WT)	10G	CWDM EML	SMF	14dB power budget	LC	Industrial

Note1: X refers to CWDM Wavelength, from 1470nm to 1610nm

\*The product image only for reference purpose.



#### CWDM\* Wavelength (0~70°C)

Band	Nomenclature	Wavelength(nm)				
Dana	Nomenciature	Min.	Typ.       Max.         1470       1477.5         1490       1497.5         1510       1517.5         1530       1537.5         1550       1557.5         1590       1597.5         1610       1617.5	Max.		
	1470	1464	1470	1477.5		
S-band Short	1490	1484	1490	1497.5		
Wavelength	1510	1504	1510	1517.5		
	1530	1524	1530	1537.5		
C-band Conventional	1550	1544	1550	1557.5		
	1570	1564	1570	1577.5		
L-band Long Wavelength	1590	1584	1590	1597.5		
	1610	1604	1610	1617.5		

CWDM\*: 8 Wavelengths from 1470nm to 1610nm, each step 20nm.

#### **Regulatory Compliance\***

Product Certificate	Certificate Number	Applicable Standard
		EN 60950-1:2006+A11+A1+A12+A2
TUV	R50135086	EN 60825-1:2014
		EN 60825-2:2004+A1+A2
1.11	E917997	UL 60950-1
UL	E317337	CSA C22.2 No. 60950-1-07
		EN 55032:2012
		EN 55032:2015
	AE 50384 190 0001	EN 55024:2010
		EN 55024:2010+A1
'FCC	WTF14F0514417E	47 CFR PART 15 OCT., 2013
FDA	/	CDRH 1040.10
ROHS	/	2011/65/EU

\*: The above certificate number updated to June 2018, because some certificate will be updated every year, such as FDA and ROHS. For the latest certification information, please check with Data Controls.

### **Product Description**

The JCxxxx-XFP-LC.S40 series optical transceiver is designed for fiber communications application such as 10G Ethernet (10GBASE-ER/EW) and 10G Fiber Channel (1200-SM-LL-L), which fully compliant with the specification of XFP MSA Rev 4.5.

This module is designed for single mode fiber and operates at a nominal wavelength of CWDM wavelength. There are eight center wavelengths available from 1470nm to 1610nm, with each step 20nm. A guaranteed optical link budget of 14dB is offered.

The module is with the XFP 30-pin connector to allow hot plug capability. Only single 3.3V power



# **XFP Series**

supply is needed. The optical output can be disabled by LVTTL logic high-level input of TX\_DIS. Loss of signal (RX\_LOS) output is provided to indicate the loss of an input optical signal of receiver. This module provides digital diagnostic functions via a 2-wire serial interface as defined by the XFP MSA Rev 4.5.

### **Absolute Maximum Ratings**

Parameter	Symbol		Min	Max	Unit
Maximum Supply Voltage	Vcc		-0.5	4.0	V
Storage Temperature	Ts		-40	85	°C
Case Operating	т	JCxxxx-XFP-LC.S40	0	70	°C
Temperature	IC	JCxxxx-XFP-LC.S40(WT)	-40	85	°C

#### **Recommend Operating Condition**

Parameter		Symbol		Typical	Max	Units
Operating Temperature	т.	JCxxxx-XFP-LC.S40	0		70	°C
	IC	JCxxxx-XFP-LC.S40(WT)	-40		85	°C
Supply Voltage 1	Vcc3		3.13	3.3	3.45	V
Supply Voltage 2	Vcc5		4.75	5	5.25	V
Supply Current-Vcc3 supply		lcc3			300	mA
Supply Current-Vcc5 supply		lcc5			750	mA
Module Total Power		Р			3.5	W

#### **Electrical Characteristics**

Parameter	Symbol	Min	Typical	Max	Unit	Note
	Т	ransmitter				
Input Differential Impedance	Rin		100		Ω	1
Differential Data Input Swing	Vin, pp	180		820	mV	
Transmit Disable Voltage	V <sub>DIS</sub>	2.0		Vcc	V	
Transmit Enable Voltage	$V_{\text{EN}}$	GND		GND+ 0.8	V	
Transmit Disable Assert Time				10	us	
		Receiver				
Differential Data Output Swing	Vout, pp	340	650	850	mV	
Data Output Rise Time	tr			38	ps	2
Data Output Fall Time	tf			38	ps	2
LOS Fault	V <sub>LOS fault</sub>	$V_{cc-0.5}$		$V_{ccHOST}$	V	3
LOS Normal	VLOS norm	GND		GND+0.5	V	3
Power Supply Rejection	PSR		See Note	e 4 below		4

#### Notes:

- 1. After internal AC coupling.
- 2. 20 80 %.
- 3. Loss of Signal is open collector to be pulled up with a 4.7k 10kohm resistor to 3.15 3.6V. Data Controls Inc. Page 3 of 10



Logic 0 indicates normal operation; logic 1 indicates no signal detected.

4. Reference the Section 2.7 of the XFP MSA Rev 4.5.

#### **Optical Characteristics**

Parameter	Symbol	Min	Typical	Max	Unit	Note
	Tr	ansmitter				
Optical Modulation Amplitude	Рома	-1		+4.4	dBm	1
Output Opt. Pwr: 9/125 SMF	Pout	-1		+4.0	dBm	
Optical Extinction Ratio	ER	8.2			dB	
Optical Wavelength	λ	λc–6	λс	λc+7.5	nm	2
-20dB Spectrum Width	Δλ			1	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Path Penalty	Рр			2.5	dB	
Average Launch Power of OFF Transmitter	$P_{OFF}$			-30	dBm	
TX Jitter	ТХj	Per 802.3ae requirements				
Relative Intensity Noise	RIN		-128			
		Receiver				
Receiver Sensitivity @ 10.3125Gb/s	Pmin			-15	dBm	3
Maximum Input Power	Pmax	+0.5			dBm	
Optical Center Wavelength	λ	1260		1620	nm	
Receiver Reflectance	Rrf			-12	dB	
LOS De-Assert	$LOS_D$			-17	dBm	
LOS Assert	LOSA	-29			dBm	
LOS Hysteresis		1			dB	

Notes:

- 1. Output is coupled into a 9/125µm SMF.
- 2. ITU-T G.694.2 CWDM wavelength from 1470nm to 1610nm, each step 20nm.
- 3. Average received power; BER less than 1E-12 and PRBS 2<sup>31</sup>-1 test pattern.

#### **Pin Descriptions**

Pin	Logic	Symbol	Name/Description	Notes
1		GND	Module Ground	1
2		VEE5	Optional –5.2 Power Supply – Not Required	
			Module De-select; When held low allows the	
3	LVTTL-I	Mod-Desel	module to respond to 2-wire serial interface	
			commands	
			/Interrupt; Indicates presence of an important	
4	LVTTL-O	/Interrupt	condition which can be read over the serial 2-wire	2
			interface	



# **XFP Series**

3LVTL-IIA_DISturned off6VCC5+5 Power Supply17GNDModule Ground18VCC3+3.3V Power Supply99VCC3+3.3V Power Supply110LVTTL-ISCLSerial 2-wire interface clock line211LVTTL-0Mod_AbsModule Absent; Indicates module is not present. Grounded in the module.212LVTTL-0Mod_AbsReceiver Loss of Signal indicator213LVTTL-0RX_LOSReceiver Loss of Signal indicator214LVTTL-0RD-Receiver inverted data output116GNDModule Ground117CML-0RD-Receiver inverted data output118CML-0RD+Receiver inverted data output120VCC2+1.8V Power Supply – Not required121LVTTL-IP_Down/RReset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.322VCC2+1.8V Power Supply – Not required323GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128C	5			Transmitter Disable; Transmitter laser source	
6VCC5+5 Power Supply7GNDModule Ground18VCC3+3.3V Power Supply99VCC3+3.3V Power Supply210LVTTL-ISCLSerial 2-wire interface clock line211LVTTL-0SDASerial 2-wire interface data line212LVTTL-0Mod_AbsModule Absent; Indicates module is not present. Grounded in the module.213LVTTL-0Mod_NRModule Not Ready;214LVTTL-0RX_LOSReceiver Loss of Signal indicator215GNDModule Ground116GNDModule Ground117CML-0RD-Receiver inverted data output18CML-0RD+Receiver non-inverted data output19GNDModule Ground120VCC2+1.8V Power Supply – Not required21LVTTL-IP_Down/RReset; The falling edge initiates a module reset22VCC2+1.8V Power Supply – Not required123GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK+Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter non-inverted data input29CML-I<	5			turned off	
7     GND     Module Ground     1       8     VCC3     +3.3V Power Supply       9     VCC3     +3.3V Power Supply       10     LVTTL-I     SCL     Serial 2-wire interface clock line     2       11     LVTTL-O     SDA     Serial 2-wire interface data line     2       12     LVTTL-O     Mod_Abs     Module Absent; Indicates module is not present. Grounded in the module.     2       13     LVTTL-O     Mod_NR     Module Absent; Indicates module is not present. Grounded in the module.     2       14     LVTTL-O     Mod_NR     Module Absent; Indicates module is not present. Grounded in the module.     2       15     GND     Module Absent; Indicates module is not present. Grounded in the module.     2       15     GND     Module Ground     1       16     GND     Module Ground     1       17     CML-O     RD+     Receiver inverted data output     1       18     CML-O     RD+     Receiver non-inverted data output     1       19     GND     Module Ground     1     1       20     VCC2     +1.8V Power Supply – Not required     1	6		VCC5	+5 Power Supply	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	7		GND	Module Ground	1
9VCC3 $+3.3V$ Power Supply10LVTTL-ISCLSerial 2-wire interface clock line211LVTTL-ISDASerial 2-wire interface data line212LVTTL-OMod_AbsModule Absent; Indicates module is not present. Grounded in the module.213LVTTL-OMod_NRModule Not Ready;214LVTTL-ORX_LOSReceiver Loss of Signal indicator215GNDModule Ground116GNDModule Ground117CML-ORD+Receiver non-inverted data output18CML-ORD+Receiver non-inverted data output19GNDModule Ground120VCC2+1.8V Power Supply – Not required21LVTTL-IP_Down/RReset; The falling edge initiates a module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset22VCC2+1.8V Power Supply – Not required223GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK-Reference Clock non-inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter non-inverted data input30GNDModule Ground1	8		VCC3	+3.3V Power Supply	
10LVTTL-ISCLSerial 2-wire interface clock line211LVTTL- VOSDASerial 2-wire interface data line212LVTTL-OMod_AbsModule Absent; Indicates module is not present. Grounded in the module.213LVTTL-OMod_NRModule Absent; Indicates module is not present. Grounded in the module.214LVTTL-OMod_NRModule Not Ready;215GNDModule Ground116GNDModule Ground117CML-ORD-Receiver inverted data output118CML-ORD+Receiver non-inverted data output119GNDModule Ground120VCC2+1.8V Power Supply – Not required121LVTTL-IP_Down/R STPower Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.322VCC2+1.8V Power Supply – Not required323GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK+Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input29	9		VCC3	+3.3V Power Supply	
11       LVTTL- I/O       SDA       Serial 2-wire interface data line       2         12       LVTTL-O       Mod_Abs       Module Absent; Indicates module is not present. Grounded in the module.       2         13       LVTTL-O       Mod_NR       Module Not Ready;       2         14       LVTTL-O       RX_LOS       Receiver Loss of Signal indicator       2         16       GND       Module Ground       1       1         17       CML-O       RD       Receiver inverted data output       1         18       CML-O       RD+       Receiver non-inverted data output       1         19       GND       Module Ground       1       1         20       VCC2       +1.8V Power Supply – Not required       1         21       LVTTL-I       P_Down/R       Power Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.       2         22       VCC2       +1.8V Power Supply – Not required       3         23       GND       Module Ground       1         24       PECL-I       RefCLK+       Reference Clock non-inverte	10	LVTTL-I	SCL	Serial 2-wire interface clock line	2
12LVTTL-OMod_AbsModule Absent; Indicates module is not present. Grounded in the module.213LVTTL-OMod_NRModule Not Ready;214LVTTL-ORX_LOSReceiver Loss of Signal indicator215GNDModule Ground116GNDModule Ground117CML-ORD-Receiver inverted data output118CML-ORD+Receiver non-inverted data output119GNDModule Ground120VCC2+1.8V Power Supply – Not required21LVTTL-IP_Down/RPower Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset21LVTTL-IReference Clock non-inverted input, AC coupled122VCC2+1.8V Power Supply – Not required23GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK+Reference Clock inverted input, AC coupled on the host board – Not required325PECL-IRefCLK+Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input129CML-ITD+Transmitter non-inverted data input130GND<	11	LVTTL- I/O	SDA	Serial 2-wire interface data line	2
12LVTTL-0Mod_NRGrounded in the module.213LVTTL-0Mod_NRModule Not Ready;214LVTTL-0RX_LOSReceiver Loss of Signal indicator215GNDModule Ground116GNDModule Ground117CML-0RD-Receiver inverted data output118CML-0RD+Receiver non-inverted data output119GNDModule Ground120VCC2+1.8V Power Supply – Not required21LVTTL-IP_Down/Redge of P_Down initiates a module in the low power stand-by mode and on the falling edge of P_Down initiates a complete reset of the module including the 2-wire serial interface, 	12		Mod Abs	Module Absent; Indicates module is not present.	2
13LVTTL-0Mod_NRModule Not Ready;214LVTTL-0RX_LOSReceiver Loss of Signal indicator215GNDModule Ground116GNDModule Ground117CML-0RD-Receiver inverted data output118CML-0RD+Receiver non-inverted data output119GNDModule Ground120VCC2+1.8V Power Supply – Not required21LVTTL-IP_Down/Redge of P_Down initiates a module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset21LVTTL-IP_Down/RReset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.322VCC2+1.8V Power Supply – Not required323GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK-Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input29CML-ITD+Transmitter non-inverted data input30GNDModule Ground1	12	EVITE-0	Mod_Ab3	Grounded in the module.	Z
14LVTTL-ORX_LOSReceiver Loss of Signal indicator215GNDModule Ground116GNDModule Ground117CML-ORD-Receiver inverted data output18CML-ORD+Receiver non-inverted data output19GNDModule Ground120VCC2+1.8V Power Supply – Not required21LVTTL-IP_Down/RPower Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset22VCC2+1.8V Power Supply – Not required23GNDReset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.24PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required25PECL-IRefCLK-Reference Clock inverted input, AC coupled on the host board – Not required26GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input29CML-ITD+Transmitter non-inverted data input30GNDModule Ground1	13	LVTTL-O	Mod_NR	Module Not Ready;	2
15GNDModule Ground116GNDModule Ground117CML-0RD-Receiver inverted data output18CML-0RD+Receiver non-inverted data output19GNDModule Ground120VCC2+1.8V Power Supply – Not required21LVTTL-IP_Down/RPower Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset21LVTTL-ISTReset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.22VCC2+1.8V Power Supply – Not required23GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK-Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input129CML-ITD+Transmitter non-inverted data input130GNDModule Ground11	14	LVTTL-O	RX_LOS	Receiver Loss of Signal indicator	2
16GNDModule Ground117CML-ORD-Receiver inverted data output118CML-ORD+Receiver non-inverted data output119GNDModule Ground120VCC2+1.8V Power Supply – Not required21LVTTL-IP_Down/RPower Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset21LVTTL-IP_Down/RReset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.22VCC2+1.8V Power Supply – Not required23GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK-Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input129CML-ITD+Transmitter non-inverted data input130GNDModule Ground11	15		GND	Module Ground	1
17CML-ORD-Receiver inverted data output18CML-ORD+Receiver non-inverted data output19GNDModule Ground120VCC2+1.8V Power Supply – Not required20VCC2+1.8V Power Supply – Not required21P_Down/RPower Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset21P_Down/RReset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.22VCC2+1.8V Power Supply – Not required23GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK-Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input129CML-ITD+Transmitter non-inverted data input130GNDModule Ground11	16		GND	Module Ground	1
18CML-ORD+Receiver non-inverted data output19GNDModule Ground120VCC2+1.8V Power Supply – Not required20VCC2+1.8V Power Supply – Not required21P_Power Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset21P_Down/R STReset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.22VCC2+1.8V Power Supply – Not required23GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK-Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input129CML-ITD+Transmitter non-inverted data input130GNDModule Ground11	17	CML-O	RD-	Receiver inverted data output	
19GNDModule Ground120VCC2+1.8V Power Supply – Not required21VCC1+1.8V Power Supply – Not required21PDown/RPower Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset21P_Down/RReset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.22VCC2+1.8V Power Supply – Not required23GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK-Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input129CML-ITD+Transmitter non-inverted data input130GNDModule Ground11	18	CML-O	RD+	Receiver non-inverted data output	
20VCC2+1.8V Power Supply – Not required21P_Down/RPower Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset21P_Down/RReset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.22VCC2+1.8V Power Supply – Not required23GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK-Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input129CML-ITD+Transmitter non-inverted data input130GNDModule Ground11	19		GND	Module Ground	1
21LVTTL-IP_Down/R STPower Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset21LVTTL-IF_Down/R STReset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.22VCC2+1.8V Power Supply – Not required23GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK-Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input129CML-ITD+Transmitter non-inverted data input130GNDModule Ground11	20		VCC2	+1.8V Power Supply – Not required	
21LVTTL-IP_Down/R STthe low power stand-by mode and on the falling edge of P_Down initiates a module reset21LVTTL-ISTReset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.22VCC2+1.8V Power Supply – Not required23GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK-Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input129CML-ITD+Transmitter non-inverted data input130GNDModule Ground1				Power Down; When high, places the module in	
21LVTTL-IP_Down/R STedge of P_Down initiates a module resetSTSTReset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.22VCC2+1.8V Power Supply – Not required23GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK-Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input129CML-ITD+Transmitter non-inverted data input130GNDModule Ground1				the low power stand-by mode and on the falling	
21LVTTL-1STReset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.22VCC2+1.8V Power Supply – Not required23GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK-Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input129CML-ITD+Transmitter non-inverted data input130GNDModule Ground11	21		P_Down/R	edge of P_Down initiates a module reset	
of the module including the 2-wire serial interface, equivalent to a power cycle.22VCC2+1.8V Power Supply – Not required23GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK-Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input129CML-ITD+Transmitter non-inverted data input130GNDModule Ground1	21		ST	Reset; The falling edge initiates a complete reset	
22VCC2+1.8V Power Supply – Not required23GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK-Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input129CML-ITD+Transmitter non-inverted data input130GNDModule Ground1				of the module including the 2-wire serial interface,	
22VCC2+1.8V Power Supply – Not required23GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK-Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input129CML-ITD+Transmitter non-inverted data input130GNDModule Ground1				equivalent to a power cycle.	
23GNDModule Ground124PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK-Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input129CML-ITD+Transmitter non-inverted data input130GNDModule Ground1	22		VCC2	+1.8V Power Supply – Not required	
24PECL-IRefCLK+Reference Clock non-inverted input, AC coupled on the host board – Not required325PECL-IRefCLK-Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input129CML-ITD+Transmitter non-inverted data input130GNDModule Ground1	23		GND	Module Ground	1
25PECL-IRefCLK-Reference Clock inverted input, AC coupled on the host board – Not required326GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input129CML-ITD+Transmitter non-inverted data input130GNDModule Ground1	24	PECL-I	RefCLK+	Reference Clock non-inverted input, AC coupled on the host board – Not required	3
26GNDModule Ground127GNDModule Ground128CML-ITD-Transmitter inverted data input129CML-ITD+Transmitter non-inverted data input130GNDModule Ground1	25	PECL-I	RefCLK-	Reference Clock inverted input, AC coupled on the host board – Not required	3
27GNDModule Ground128CML-ITD-Transmitter inverted data input29CML-ITD+Transmitter non-inverted data input30GNDModule Ground1	26		GND	Module Ground	1
28CML-ITD-Transmitter inverted data input29CML-ITD+Transmitter non-inverted data input30GNDModule Ground1	27		GND	Module Ground	1
29CML-ITD+Transmitter non-inverted data input30GNDModule Ground1	28	CML-I	TD-	Transmitter inverted data input	
30 GND Module Ground 1	29	CML-I	TD+	Transmitter non-inverted data input	
	30		GND	Module Ground	1

#### Notes:

1. Module circuit ground is isolated from module chassis ground within the module.

- 2. Open connect should be pulled up with 4.7k 10k ohm on host board to a voltage between 3.15V and 3.6V.
- 3. A Reference Clock input is not required.



### Host Board Connector Pin Out



**Diagram of Host Board Connector Block Pin Numbers and Name** 

#### **General Specifications**

Parameter	Symbol	Min	Typical	Max	Units	Note
Bit Rate	BR	9.95		11.1	Gb/s	
Bit Error Ratio	BER			10 <sup>-12</sup>		1

Notes:

1. Tested 9.95G with 2<sup>31</sup> – 1 PRBS pattern.

#### **Digital Diagnostic Functions**

Data Controls's Small Form Factor 10Gbps (XFP) transceiver is compliant with the current XFP Multi-Source Agreement (MSA) Specification Rev 4.5.

As defined by the XFP MSA, Data Controls XFP transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current
- Transmitted optical power
- Received optical power
- Aux Monitoring

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range. The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller inside the transceiver, which is accessed through the 2-wire serial interface. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 00h to the maximum address of the memory.



#### **Recommended Host Board Power Supply Circuit**







### **Recommended High-Speed Interface Circuit**

#### **Mechanical Specifications**

Data Controls's XFP transceivers are compliant with the dimensions defined by the XFP Multi-Sourcing Agreement (MSA).



\*This 2D drawing only for reference, please check with Data Controls before ordering.



## Eye Safety

This single-mode transceiver is a Class 1 laser product. It complies with IEC-60825 and FDA 21 CFR 1040.10 and 1040.11. The transceiver must be operated within the specified temperature and voltage limits. The optical ports of the module shall be terminated with an optical connector or with a dust plug.

#### **Obtaining Document**

You can visit our website: http://www.dci.jp

Or contact Data Controls Inc. Listed at the end of the documentation to get the latest documents.

#### Notice:

Data Controls reserves the right to make changes to or discontinue any optical link product or service identified in this publication, without notice, in order to improve design and/or performance. Applications that are described herein for any of the optical link products are for illustrative purposes only. Data Controls makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

#### **Contact:**

E-mail:info@dci.jp http://www.dci.jp